REMARKS/ARGUMENT

Claims 1-21 are pending in the application. Claims 1-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Eikemeyer (U.S. Patent No. 6,694,425) ("Eikemeyer"). The Title is amended to bring in more in line with Applicants' disclosure. Claims 1 ,5, 10, 15 and 16 are amended to put them into better form.

Applicants respectfully submit that the cited references do not teach, suggest or disclose "[a] method comprising: ... flushing an instruction from said first thread from a pipeline of said processing system if data is to be loaded from said memory device before executing said instruction" (e.g., as described in claim 1).

The Office Action asserts that Eikemeyer teaches flushing an instruction from the thread of a pipeline of said processing system when data is to be loaded from [a] memory device before executing the instruction. *See* Office Action dated 12/21/05, page 4, paragraph 6. Applicants respectfully disagree. The Office Action cites column 1, lines 6-12; column 6, lines 18-26 and column 11, lines 41-49. Column 1, lines 6-12 state:

> The present invention relates in general to an improved data processing system and in particular to an improved system and method for switching threads of execution when execution of a thread is stalled in the dispatch stage of a multithread pipelined processor and flushing the stalled thread from earlier stages of pipeline.

Applicants agree with the Office Action's assertion that this section includes the generic description of an instruction of a thread being flushed. *See* paragraph 6, line 10. The cited section describes an improved system for switching threads when execution of a thread is stalled in a multithreaded pipelined processor and flushing the stalled thread from earlier stages of a pipeline.

However, this generic disclosure of the purpose behind the Eikemeyer reference does not disclose "...flushing an instruction from said first thread from a pipeline of said processing

system *if data is to be loaded from [a] memory device before executing said instruction*" (e.g., as described in claim 1). In order to be a proper §102(e) rejection, the reference must describe the limitations as found in claim 1. The above cited section does not.

Next, the Office Action cites column 6, lines 18-26 of Eikemeyer, which state:

> ... flush decode logic to determine if the thread having the stalled instruction has a previous flush condition, a dispatch flush mechanism to flush the thread having the stalled instruction from the fetch stage, the decode stage, and the dispatch stage if no other previous flush condition exists or if the previous flush condition has a lower priority than the stalled instruction so that the processor can process another of the independent threads of execution with the processor pipeline.

The cited section of Eikemeyer is intended to describe a) flush decode logic used to make the conditional determination as to whether there is a flush condition associated with a stalled instruction and b) a dispatch flush mechanism to flush the thread with the instruction.

Applicants submit that the cited sections fail to disclose the relevant limitations. The cited reference does not describe "...flushing an instruction from said first thread from a pipeline of said processing system *when data is to be loaded from [a] memory device before executing said instruction*" (e.g., as described in claim 1). Therefore, the cited section is inadequate to support a proper §102(e) rejection of claim 1.

The Office Action further cites column 11, lines 41-49 of Eikemeyer. The cited section states:

> The dispatch flush causes that thread having an instruction that is stalled at the dispatch unit 220 to be flushed from the instruction fetch and decode portions of the pipeline and all other portions of the processor's pipeline up to and including the dispatch unit 220. A flush control signal 262 causes both a dispatch flush and a normal flush/refetch 238 to flush instructions of a particular thread from the dispatch unit 220 and earlier pipeline stages.

The cited section describes flushing a thread (including an instruction) from the pipeline and the use of a flush control signal to do so. Applicants submit this section fails to support a proper §102(e) rejections for similar to those reasons detailed above. The cited section does not

describe flushing an instruction when data *is to be loaded from a memory device before executing the instruction*, as specifically recited in the claim 1.

Therefore, since each and every limitations is not found in the cited reference, the cited reference cannot adequately form the basis of a proper 35 U.S.C. §102(e) rejection of independent claim 1. Independent claims 5, 10, and 16 contain substantively similar limitations and therefore are also allowable for similar reasons. Claims 2-4, 6-9, 11-15 and 17-21 depend from allowable independent claims 1, 5, 10 and 16, and therefore are in condition for allowance as well.

For at least the above reasons, Applicants respectfully submit that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (408) 975-7500 to discuss any matter concerning this application. The Office is hereby authorized to charge any additional fees or credit any overpayments to Deposit Account No. **11-0600**.

Respectfully submitted,

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